AMENDMENTS TO THE CLAIMS:

1. (Currently amended) A semiconductor device comprising:

a tristate buffer circuit ~~including~~ comprising, on an output stage, ~~at least~~ a first transistor for pull-up driving and a second transistor for pull-down driving, in which, when a control signal is of a value indicating an enable state, an output is set to a high level or to a low level, depending on a data signal, and in which, when the control signal is of a value indicating a disable state, said first and second transistors are both turned off to set the output in a high impedance ~~state, said semiconductor device further comprising~~ state;

a control circuit for performing control ~~for speeding~~ to speed up the transition from an on-state to an off-state of said first transistor when said control signal is switched from said enable state to said disable state;

a logic circuit for receiving said data signal and said control signal as inputs and outputting a first signal for controlling the on/off state of said first transistor; and

a transmission gate comprising a third transistor, said third transistor being turned on when said control signal is of a value indicating the enable state and receiving said first signal output from said logic circuit to transfer said first signal to a control terminal of said first transistor, said third transistor being turned off when said control signal is of the value indicating the disable state, wherein:

said control circuit comprises a circuit for receiving said control signal and delaying the timing of changing over the state of said third transistor of said transmission gate from an on-state to an off-state at the time of switching the state of said control signal from the enable state to the disable state; and

during the time said third transistor is on, when the state of said control signal is switched from the enable state to the disable state, said transmission gate transfers the level of said first signal output from said logic circuit for turning off said first transistor to a control terminal of said first transistor to speed up the transition from the on-state to the off-state of said first transistor.

2. (Currently amended) The semiconductor device as defined in claim 1, wherein said control circuit ~~includes~~ comprises a circuit which, when said control signal is of a value indicating the enable state, and a signal determining the on/off state of said first transistor is of a level indicating the on-state of said first transistor, performs control to shorten the time until said signal determining the on/off state of said first transistor gets to a level ~~of~~ turning off said first transistor at the time of switching of said control signal from said enable state to said disable state.

3. (Canceled)

4. (Currently amended) The semiconductor device as defined in claim 1, wherein said control circuit ~~includes~~ comprises a circuit for rendering a path across the control terminal of said first transistor and the power supply electrically conductive responsive to said control signal to set the control terminal of said first transistor to a voltage which turns off said first transistor.

5. (Currently amended) A ~~The~~ semiconductor device, ~~as defined in claim 1, further~~ comprising:

a tristate buffer circuit comprising, on an output stage, ~~at least~~ a first transistor for pull-up driving and a second transistor for pull-down driving, in which, when a control signal is of a value indicating an enable state, an output is set to a high level or to a low level, depending on a data signal, and in which, when the control signal is of a value indicating a disable state, said first and second transistors are both turned off to set the output in a high impedance state;

a control circuit for performing control to speed up the transition from an on-state to an off-state of said first transistor when said control signal is switched from said enable state to said disable state;

a first logic circuit for receiving said data signal and said control signal as inputs and for outputting a first signal controlling the on/off state of said first transistor; and

a transmission gate connected across an output terminal of said first logic circuit and the control terminal of said first transistor; wherein:

~~wherein~~ said first logic circuit outputs a second logic value as said first signal, when said control signal indicates the enable state and said data signal is of a first logic value, and outputs the first logic value, as said first signal, without dependency on the value of said data signal, when said control signal is of a value indicating the disable state;

~~wherein~~ said first transistor is turned on and off when the control terminal of said first transistor is of the second logic value and of the first logic value, respectively;

~~wherein~~ said transmission gate ~~includes~~ comprises a third transistor controlled to be

on when said control signal is in the enable state;

~~wherein~~ said control circuit ~~includes~~ comprises a timing adjustment circuit for receiving said control signal and delaying the transition timing from the enable state to the ~~disabled~~ disable state of said control signal to output the delayed signal as a second control signal; and

~~wherein~~ said third transistor ~~of said transmission gate~~ is changed over from an on-state to an off-state based on transition from the enable state to the disable state of said second control signal output from said timing adjustment circuit.

6. (Currently amended) The semiconductor device as defined in claim 5, wherein said timing adjustment circuit ~~includes~~ comprises a delay circuit for receiving and delaying said control signal a preset time to output the delayed signal.

7. (Currently amended) The semiconductor device as defined in claim 5, wherein said timing adjustment circuit ~~includes~~ comprises:

a delay circuit for receiving said control signal and delaying the control signal a preset time to output the delayed signal; and

a second logic circuit for receiving said control signal and an output signal of said delay circuit and delaying for a preset time the transition from the enable state to the disable state of said control signal to output the delayed signal as said second control signal.

8. (Currently amended) A ~~The~~ semiconductor device, ~~as defined in claim 1, further~~

comprising:

a tristate buffer circuit comprising, on an output stage, ~~at least~~ a first transistor for pull-up driving and a second transistor for pull-down driving, in which, when a control signal is of a value indicating an enable state, an output is set to a high level or to a low level, depending on a data signal, and in which, when the control signal is of a value indicating a disable state, said first and second transistors are both turned off to set the output in a high impedance state;

a control circuit for performing control to speed up the transition from an on-state to an off-state of said first transistor when said control signal is switched from said enable state to said disable state;

a first logic circuit for receiving said data signal and said control signal as inputs and outputting a first signal controlling the on/off state of said first transistor; and

a transmission gate connected across an output terminal of said first logic circuit and the control terminal of said first transistor; wherein:

~~wherein~~ said first logic circuit outputs a second logic value as said first signal, when said control signal indicates the enable state and said data signal is of a first logic value, and outputs the first logic value, as said first signal, without dependency on the value of said data signal, when said control signal is of a value indicating the disable state;

~~wherein~~ said first transistor is turned on and off when the control terminal of said first transistor is of the second logic value and of the first logic value, respectively;

~~wherein~~ said transmission gate ~~includes~~ comprises a third transistor controlled to be on when said control signal is in the enable state;

~~wherein~~ said control circuit ~~includes~~ comprises a further circuit connected across the control terminal of said first transistor and the power supply, said further circuit, when said control signal is of a value indicating the enable state, rendering a path between said power supply and a control terminal node of said first transistor to an electrically non-conductive state; said further circuit, when said control signal is of a value indicating the disable state, rendering the path between said power supply and ~~a~~ the control terminal node of said first transistor to an electrically conductive state to set the voltage of the control terminal of said first transistor to a level ~~of~~ turning off said first transistor.

9. (Currently amended) The semiconductor device as defined in claim 5, wherein said control circuit further ~~includes~~ comprises a further circuit connected across the control terminal of said first transistor and the power supply; wherein:

~~wherein~~ said further circuit, when said control signal is of a value indicating the enable state, renders a path between said power supply and a control terminal node of said first transistor to an electrically non-conductive state; and

~~wherein~~ said further circuit, when said control signal is of a value indicating the disable state, renders the path between said power supply and a control terminal node of said first transistor to an electrically conductive state to set the voltage of the control terminal of said first transistor to a level ~~of~~ turning off said first transistor.

10. (Currently amended) A ~~The~~ semiconductor device, ~~as defined in claim 1, further~~ comprising:

a tristate buffer circuit comprising, on an output stage, ~~at least~~ a first transistor for pull-up driving and a second transistor for pull-down driving, in which, when a control signal is of a value indicating an enable state, an output is set to a high level or to a low level, depending on a data signal, and in which, when the control signal is of a value indicating a disable state, said first and second transistors are both turned off to set the output in a high impedance state;

a control circuit for performing control to speed up the transition from an on-state to an off-state of said first transistor when said control signal is switched from said enable state to said disable state;

a ~~second~~ logic circuit for receiving said control signal and said data signal as inputs and outputting a ~~second~~ further signal controlling the on/off state of said second transistor; an output terminal of said ~~second~~ logic circuit being connected to a control circuit of said second transistor; wherein:

~~wherein~~ said ~~second~~ logic circuit, when said control signal indicates an enable state and said data signal assumes first and second logic values, outputs, as said ~~second~~ further signal, an output signal causing said second transistor to be turned off and on, respectively; and

~~wherein~~ said ~~second~~ logic circuit, when said control signal indicates a disable state, outputs an output signal causing said second transistor to be turned off, as said ~~second~~ further signal, without dependency on said data signal.

11. (Currently amended) A ~~The~~ semiconductor device, ~~as defined in claim 1, further~~

comprising:

a tristate buffer circuit comprising, on an output stage, ~~at least~~ a first transistor for pull-up driving and a second transistor for pull-down driving, in which, when a control signal is of a value indicating an enable state, an output is set to a high level or to a low level, depending on a data signal, and in which, when the control signal is of a value indicating a disable state, said first and second transistors are both turned off to set the output in a high impedance state;

a control circuit for performing control to speed up the transition from an on-state to an off-state of said first transistor when said control signal is switched from said enable state to said disable state;

a pad connected to an output node of said first transistor and ~~composing~~ comprising an output of said tristate buffer circuit; and

a bypass circuit connected across the control terminal of said first transistor and ~~an~~ the output node of said first transistor for forming a bypass across the output node of said first transistor and said control terminal of said first transistor, when the voltage applied to said pad is equal to or higher than the power supply voltage of said tristate buffer.

12. (Currently amended) The semiconductor device as defined in claim 5, further comprising:

a pad ~~composing~~ comprising an output of said tristate buffer circuit;

a fourth transistor having a control terminal supplied with the power supply potential and ~~composing~~ comprising said transmission gate, said fourth transistor being of ~~the~~ a second

conductivity type, ~~(termed a 'second conductivity type')~~ opposite to ~~the~~ a first conductivity type of said third transistor ~~(termed a 'first conductivity type')~~ which is turned on when said second control signal from said timing adjustment circuit is of a value indicating the enable state;

a series circuit ~~including~~ comprising a fifth transistor of the second conductivity type, and having a control gate supplied with the power supply potential, and a sixth transistor of the second conductivity type, controlled to an off-state and to an on-state when said second control signal from said timing adjustment circuit is of a value indicating the enable state and of a value indicating the disable state, respectively, said series circuit connected between the control terminal of said third transistor and said pad; and

a seventh transistor of the first conductivity type having a control terminal supplied with the power supply potential, between the control terminal of said third transistor and said pad, in parallel with said series circuit.

13. (Currently amended) The semiconductor device as defined in claim 5, further comprising:

a pad ~~composing~~ comprising an output of said tristate buffer circuit;

a fourth transistor having a control terminal supplied with the power supply potential, and ~~composing~~ comprising said transmission gate, said fourth transistor being of ~~the~~ a second conductivity type, ~~(termed a 'second conductivity type')~~ opposite to ~~the~~ a first conductivity type of said third transistor ~~(termed a 'first conductivity type')~~ which is turned on when said second control signal from said timing adjustment circuit is of a value indicating the enable

state;

a fifth transistor of the second conductivity type, between the control terminal of said third transistor and said pad, said fifth transistor being controlled to be off and on when said second control signal from said timing adjustment circuit is of a value indicating the enable state and the disable state, respectively;

a sixth transistor of the first conductivity type having a control terminal supplied with the power supply potential and connected between the control terminal of said third transistor and said pad, in parallel with said fifth transistor.

14. (Currently amended) The semiconductor device as defined in claim ~~8~~ 34, further comprising:

a pad ~~composing~~ comprising an output of said tristate buffer circuit;

a fourth transistor having a control terminal supplied with the power supply potential, and ~~composing~~ comprising said transmission gate, said fourth transistor being of ~~the~~ a second conductivity type, ~~(termed a 'second conductivity type')~~ opposite to ~~the~~ a first conductivity type of said third transistor ~~(termed a 'first conductivity type')~~ which is turned on when said second control signal from said timing adjustment circuit is of a value indicating the enable state;

a series circuit ~~including~~ comprising a fifth transistor of the second conductivity type, having a control gate supplied with the power supply potential, and a sixth transistor of the second conductivity type, controlled to an off-state and to an on-state when said second control signal from said timing adjustment circuit is of a value indicating the enable state and

of a value indicating the disable state, respectively, said series circuit connected between the control terminal of said third transistor and said pad; and

a seventh transistor of the first conductivity type having a control terminal supplied with the power supply potential, between the control terminal of said third transistor and said pad, in parallel with said series circuit.

15. (Currently amended) The semiconductor device as defined in claim ~~8~~ 34, further comprising:

a pad ~~composing~~ comprising an output of said tristate buffer circuit;

a fourth transistor having a control terminal supplied with the power supply potential, and ~~composing~~ comprising said transmission gate, said fourth transistor being of ~~the~~ a second conductivity type, ~~(termed a 'second conductivity type')~~ opposite to ~~the~~ a first conductivity type of said third transistor ~~(termed a 'first conductivity type')~~ which is turned on when said second control signal from said timing adjustment circuit is of a value indicating the enable state;

a fifth transistor of the second conductivity type, between the control terminal of said third transistor and said pad, said fifth transistor being controlled to be off and on when said second control signal from said timing adjustment circuit is of a value indicating the enable state and the disable state, respectively;

a sixth transistor of the first conductivity type having a control terminal supplied with the power supply potential and connected between the control terminal of said third transistor and said pad, in parallel with said fifth transistor.

16. (Currently amended) a ~~The~~ semiconductor device, ~~as defined in claim 1, further~~ comprising:

a tristate buffer circuit comprising, on an output stage, ~~at least~~ a first transistor for pull-up driving and a second transistor for pull-down driving, in which, when a control signal is of a value indicating an enable state, an output is set to a high level or to a low level, depending on a data signal, and in which, when the control signal is of a value indicating a disable state, said first and second transistors are both turned off to set the output in a high impedance state;

a control circuit for performing control to speed up the transition from an on-state to an off-state of said first transistor when said control signal is switched from said enable state to said disable state;

a pad connected to an output node of said first transistor and ~~composing~~ comprising an output of said tristate buffer circuit; and

~~an eighth~~ a third transistor provided in a well region common to the well region of said first transistor or in a well region connected to the well region of said first transistor, said ~~eighth~~ third transistor being of the same conductivity type as said first transistor and having a control terminal connected to said pad;

wherein electric connection between said well region and the power supply is controlled to be in an off-state through said ~~eighth~~ third transistor when the voltage of said pad is equal to or higher than the power supply voltage of said tristate buffer circuit.

17. (Currently amended) The semiconductor device as defined in claim 5, further comprising:

a pad connected to an output node of said first transistor and ~~composing~~ comprising an output of said tristate buffer circuit; and

~~an eighth~~ a fourth transistor provided in a well region common to the well region of said first transistor or in a well region connected to the well region of said first transistor, said ~~eighth~~ fourth transistor having a control terminal connected to said pad and being of the same conductivity type as said first transistor; wherein:

~~wherein~~ the third transistor, ~~composing~~ comprising said transmission gate, is arranged in a well region common to a well region of said first transistor and/or said ~~eighth~~ fourth transistor or in a well region connected to the well regions of said first transistor and said ~~eighth~~ fourth transistor; and

wherein electric connection between said well region associated with said first, third and ~~eighth~~ fourth transistors and the power supply are controlled to be in an off-state through said ~~eighth~~ fourth transistor when the voltage of said pad is equal to or higher than the power supply voltage of said tristate buffer circuit.

18. (Currently amended) The semiconductor device as defined in claim 16, further comprising:

a ~~ninth~~ fourth transistor of the same conductivity type as said first transistor, having the control terminal supplied with the power supply potential and connected across the control terminal and an output node of said first transistor; said ~~ninth~~ fourth transistor being

provided in a well region common to the well region of said first transistor and/or said ~~eighth~~ third transistor or in a well region connected to the well region of said first transistor and said ~~eighth~~ third transistor;

_____wherein electric connection between said well region associated with said ~~ninth~~ fourth transistor and the power supply is controlled to be in an off-state through said ~~eighth~~ third transistor when the voltage of said pad is equal to or higher than the power supply voltage of said tristate buffer circuit.

19. (Currently amended) The semiconductor device as defined in claim 5, further comprising:

a ~~tenth~~ fourth transistor between the control terminal of said third transistor of said transmission gate and a second power supply, said ~~tenth~~ fourth transistor having a control terminal supplied with said second control signal output from said timing adjustment circuit and being turned on and off when said second control signal is of a value indicating the enable state and the disable state, respectively.

20. (Currently amended) The semiconductor device as defined in claim 8, further comprising

a ~~tenth~~ fourth transistor between the control terminal of said third transistor of said transmission gate and a second power supply, said ~~tenth~~ fourth transistor having a control terminal supplied with said control signal and being turned on and off when said control signal is of a value indicating the enable state and the disable state, respectively.

21. (Currently amended) The semiconductor device as defined in claim 19, further comprising

~~an eleventh~~ a fifth transistor connected across the control terminal of said third transistor of said transmission gate and an output node of said ~~tenth~~ fourth transistor and having a control terminal supplied with the power supply potential.

22. (Currently amended) The semiconductor device as defined in claim 1, further comprising:

a ~~twelfth~~ fourth transistor between a pad ~~composing~~ comprising an output of said tristate buffer circuit and an output of said second transistor, and having a control terminal supplied with the power supply potential.

23. (Currently amended) The semiconductor device as defined in claim ~~3~~ 1, further comprising:

a pad ~~composing~~ comprising an output of said tristate buffer circuit; ~~wherein~~

wherein said control circuit ~~including~~ comprises a circuit for receiving a signal reflecting the voltage of said pad and said control signal to perform control to cause said third transistor, ~~composing~~ comprising said transmission gate, to be transiently turned on, during transition from said enable state to the disable state of said control signal, when said signal reflecting the pad voltage indicates a high level voltage.

24. (Currently amended) The semiconductor device as defined in claim 5, further comprising:

a one-shot pulse generating circuit for receiving said control signal and detecting the switching from the enable state to the disable state of said control signal to generate a one-shot pulse signal of a preset pulse width; and

a ~~thirteenth~~ fourth transistor connected across an output node of said tristate buffer circuit and a second power supply for receiving an output signal of said one-shot pulse generating circuit, said ~~thirteenth~~ fourth transistor being turned on during ~~the~~ a period ~~as~~ determined by the pulse width of said one-shot pulse signal.

25. (Currently amended) A ~~The~~ semiconductor device, ~~as defined in claim 1, further~~ comprising:

a tristate buffer circuit comprising, on an output stage, ~~at least~~ a first transistor for pull-up driving and a second transistor for pull-down driving, in which, when a control signal is of a value indicating an enable state, an output is set to a high level or to a low level, depending on a data signal, and in which, when the control signal is of a value indicating a disable state, said first and second transistors are both turned off to set the output in a high impedance state;

a control circuit for performing control to speed up the transition from an on-state to an off-state of said first transistor when said control signal is switched from said enable state to said disable state;

a one-shot pulse generating circuit for receiving said control signal and detecting the

switching from the enable state to the disable state of said control signal to generate a one-shot pulse signal of a preset pulse width; and

a logic circuit for receiving said data signal and an output signal of said one-shot pulse generating circuit to generate a signal which turns on said second transistor when said data signal is of ~~the second~~ a selected logic value or when said one-shot pulse signal is active.

26. (Currently amended) The semiconductor device as defined in claim 8, wherein said control circuit ~~includes~~ comprises at least two transistors connected in series across the control terminal of said first transistor and said power supply; wherein:

one of said two transistors ~~being~~ is connected in a diode configuration;

the other ~~transistor having~~ of said two transistors has a control terminal supplied with said control signal and being turned off and on when said control signal is of a value indicating the enable state and the disable state, respectively.

27. (Currently amended) The semiconductor device as defined in claim 26, further comprising

a pad connected to an output of said tristate buffer circuit; wherein:

~~wherein~~ one of said two transistors of said control circuit is provided in a well region common to the well region of said first transistor and/or the well region of said ~~eighth~~ third transistor or in said well regions of said first transistor and said ~~eighth~~ third transistor; and

~~wherein~~ an electric connection between the power supply and said well regions of said first and third transistors and the one ~~transistor~~ of said two transistors of said control circuit is

controlled to be in an off-state through said ~~eighth~~ third transistor when the voltage of said pad is equal to or higher than the power supply voltage of said tristate buffer circuit.

28. (Currently amended) A ~~The~~ semiconductor device, ~~as defined in claim 1,~~ comprising:

a tristate buffer circuit comprising, on an output stage, ~~at least~~ a first transistor for pull-up driving and a second transistor for pull-down driving, in which, when a control signal is of a value indicating an enable state, an output is set to a high level or to a low level, depending on a data signal, and in which, when the control signal is of a value indicating a disable state, said first and second transistors are both turned off to set the output in a high impedance state;

a control circuit for performing control to speed up the transition from an on-state to an off-state of said first transistor when said control signal is switched from said enable state to said disable state;

wherein said tristate buffer circuit ~~is~~ comprises a tolerant buffer circuit capable of applying in a disable state a voltage higher than the power supply voltage of said tristate buffer circuit or than said driving power supply voltage.

29. (Currently amended) The semiconductor device as defined in claim 1, further comprising: ~~an I/O buffer circuit, including:~~

a pad connected to an output of said tristate buffer circuit; and

an input buffer connected to said pad; wherein:

~~wherein~~ said tristate buffer circuit, said pad and said input buffer ~~compose~~ comprise

an I/O buffer circuit which is set to an output mode of outputting a level corresponding to said data signal from said tristate buffer circuit to said pad when said control signal is of a value indicating the enable state; and

~~wherein~~ said I/O buffer circuit is set to an input mode of receiving a signal applied to said pad by said input buffer when said control signal is of a value indicating the disable state.

30. (Currently amended) The semiconductor device as defined in claim 29, further comprising:

a circuit connected across said pad and said input buffer for supplying a signal of the level of said power supply voltage to an input end of the input buffer when the voltage equal to or higher than the power supply voltage of said tristate buffer is applied to said pad.

31. (Currently amended) The semiconductor device as defined in claim 5, further comprising:

a pad ~~composing~~ comprising an output of said tristate buffer circuit; ~~wherein~~

wherein said timing adjustment circuit receives a signal reflecting the voltage of said pad and said control signal to perform control to cause said third transistor, ~~composing~~ comprising said transmission gate, to be transiently turned on, during transition from said enable state to the disable state of said control signal, when said signal reflecting the pad voltage indicates a high level voltage.

32. (Currently amended) The semiconductor device as defined in claim 8, further

comprising:

a pad ~~composing~~ comprising an output of said tristate buffer circuit; ~~wherein~~

wherein said control circuit ~~include~~ comprises a circuit receiving a signal reflecting the voltage of said pad and said control signal to perform control to cause said third transistor, ~~composing~~ comprising said transmission gate, to be transiently turned on, during transition from said enable state to the disable state of said control signal, when said signal reflecting the pad voltage indicates a high level voltage.

33. (Currently amended) The semiconductor device as defined in claim 9, wherein:

_____said control circuit ~~includes~~ comprises at least two transistors connected in series across the control terminal of said first transistor and said power supply;

one of said two transistors ~~being~~ is connected in a diode configuration;

_____the other ~~transistor having~~ of said two transistors has a control terminal supplied with said control signal and ~~being~~ is turned off and on when said control signal is of a value indicating the enable state and the disable state, respectively.

34. (New) The semiconductor device as defined in claim 8, wherein said control circuit comprises a timing adjustment circuit for receiving said control signal and delaying the transition timing from the enable state to the disable state of said control signal to output the delayed signal as a second control signal.